A 53-to-75-mW, 59.3-dB HRR, TV-Band White-Space Transmitter Using a Low-Frequency Reference LO in 65-nm CMOS

Ka-Fai Un, Student Member, IEEE, Pui-In Mak, Senior Member, IEEE, and Rui P. Martins, Fellow, IEEE

Abstract—A TV-band white-space transmitter covering a 16x-wide spectrum from 54 to 864 MHz is described. It features a systematic codesign between the architecture and circuits to address the harmonic-mixing problem. Specifically, it incorporates two-stage 6-/14-path harmonic-rejection mixers and low-Q passive-RC-LC filters to manage the unwanted harmonic emission fully on chip, achieving an uncalibrated harmonic rejection ratio (HRR) of minimally 59.3 dB (16 samples) for all in-/out-band harmonics. The employed 8-/16-phase LO generator is based on injection-locked 4-/8-phase correctors and even-ratio-only frequency dividers to save the LO-path power (2.5 to 14.2 mW) while lowering the required reference LO frequency (432 to 864 MHz). Without any predistortion, the EVM tested under a 64-QAM OFDM digital-TV signal is 2.9% at 96 MHz, 3.3% at 384 MHz, and 4.0% at 600 MHz. The first (second) adjacent channel leakage ratio is $-46$ dBc ($-32$ dBc) at 6 MHz (12 MHz) offset. The power consumption is 53.1 to 75.2 mW and active area is 0.93 mm² in 65-nm CMOS.

Index Terms—CMOS, harmonic rejection, multiphase local oscillator (LO) generator, OFDM, passive filter, white space applications, wideband, wireless transmitter.

I. INTRODUCTION

The scope of sharing the geographically unused white spaces in TV band (54 to 864 MHz) has led to the development of IEEE 802.22 wireless regional area network (WRAN) [1], which embodies the cognitive radio (CR) techniques to enable an opportunistic share of the spectrum [2]. To avoid causing detrimental interference to the incumbent primary users, one key challenge of such a TV-band transmitter (TX) lies on managing the unwanted harmonic emission [3] without pricey or complicated filtering modules [4].

Hard-switching mixer is one of the sources generating influential sidebands associated with the harmonics of the local oscillator (LO). Multipath mixers feature the desired integratability and wideband ability in harmonic rejection [5]. A typical differential mixer already can stem all even harmonics, while rejecting the odd ones entails additional paths. The six-path harmonic-reject mixer (6P-HRM) [6] can suppress the critical third and fifth harmonics by around 35 dB under typical 1% gain and 1° phase errors, but it is still not the whole for a TX covering a 16x-wide RF range, i.e., harmonics up to the 15th are in-band. An active tunable-LC filter [7] can be employed to extend both harmonic rejection ratio (HRR) (42 dB) and the number of rejecting harmonics (up to 15th), but the power (171 mW) is penalized to uphold the linearity, while calibration should be adopted to surmount the LC-tank variation. Although the 18-path HRM (18P-HRM) [8] is capable to reject harmonics up to the 15th (40 dB HRR) and suppress certain distortion sidebands, the enforced baseband (BB) input (18 paths, 18 phases) and LO format (18 phases, 33% duty cycle) are complicated. The former implies seven more differential digital-to-analog converters (DACs) and 14 more I/O pins than the 6P-HRM. The latter resorted from a div-by-9 ring counter draws substantial power (156 mW) and entails a high-frequency reference LO $\{L_{oref} = 9\times$RF$\}$, adding complexity to the frequency synthesis.

In fact, the constraint of high $L_{oref}$ is shared by most HRM-based architectures. For the receiver in [9], $L_{oref} = 8\times$RF is entailed for precise eight-phase LO generation, limiting its operating bandwidth (BW) between 400 to 900 MHz (albeit a 5-GHz signal-path BW). Another example is [10], the rotational 16P-HRM entails $L_{oref} = 16\times$RF, restricting its operating BW between 100 to 300 MHz while drawing considerable power (69.8 mW at 100 MHz).

This work describes a number of techniques to realize a wideband TX with high HRR achieved on chip, measuring more favorable power (53 to 75 mW) and HRR (59.3 dB) than the prior art [7], [8], while breaking the common constraint of high-frequency reference LO $\{L_{oref}\}$ in existing HRM-based architectures [7]–[10].

The remainder of this paper is organized as follows. Section II introduces the proposed TX architecture. Section III describes the principles of single-/two-stage 6P-HRM and 14P-HRM. The circuit implementation is detailed in Section IV and the experimental results are given in Section V. Finally, the conclusions are drawn in Section VI.

II. PROPOSED TX ARCHITECTURE

Fig. 1(a) depicts the proposed wideband direct-upconversion TX architecture aiming at a 60-dB HRR for all LO harmonics. The TV band is partitioned into lower (54 to 432 MHz) and...
upper (432 to 864 MHz) sub-bands. The system plan is as follows.

The lower subband is handled by a scheme: Two-Stage 14P-HRM + Passive Filtering. Unlike the single-stage HRMs [6]–[8], the two-stage HRM expanded from [9] is highly robust to the gain error by making it the product of stage errors (details are given in Section III-D). Comparing with the 18P-HRM, the 14P-HRM rejects one less harmonic (i.e., the 15th), but the requested BB inputs (four paths, four phases) and LO format (16 phases, 50% duty cycle) are much simpler. As shown in Fig. 1(b), the worst HRR happens at the lowest RF of 54 MHz. The far-out 15th harmonic at 810 MHz has an inherent attenuation of 23.5 dB and can be easily furthered by filtering. Unlike the active LC-notch filter [7], here a simple second-order passive-RC low-pass filter (LPF) is employed as the harmonic-rejection filter (HRF), having neither power nor linearity overhead. A few BW steps automatically selected with the LO bands are simple enough to enhance both in-band and out-band HRRs.

For the upper subband, it is handled by a scheme: Two-Stage 6P-HRM + Passive Filtering. As shown in Fig. 1(c), the worst HRR occurs at 432 MHz RF, locating the first uncancelled seventh harmonic at around 3 GHz which is far from the TX BW, and will be well suppressed by the HRF.

In order to band-limit the output noise spectrum and further the out-band HRR, the driver amplifier (DA) features another third-order passive-CLC LPF to serve as a band-selection filter (BSF). Both the BSF and HRF are low-Q and thereby immune to process variations.

Counting all filtering and the intrinsic decay of LO-harmonic power, the HRR requested from the two-stage 6P-HRM (14P-HRM) is relaxed to 36 dB (43 dB) for the 60-dB HRR target. This relaxation implies lower LO-phase-error requirement from the 8-/16-phase LO generator (LOG), given that the gain error has been made insignificant to the HRR under the two-stage HRMs. The principles of single-/two-stage 6P-HRM and 14P-HRM are presented next.
III. SINGLE-/TWO-STAGE 6P-HRM AND 14P-HRM

A. Single-Stage 6P-HRM and 14P-HRM

Fig. 2(a) depicts the single-ended diagram of single-stage 6P-HRM. It entails an eight-phase LOG for 45° phase shifting and a gain ratio \[ \cos(\pi/4) : 1 : \cos(\pi/4) \] between paths. The limitation of 6P-HRM is that mainly the third, fifth, 11th, and 13th harmonics are rejected. Alternatively, the single-stage 14P-HRM [Fig. 2(b)] rejects harmonics up to the 13th. It entails a 16-phase LO for 22.5° phase shifting, and a gain ratio \[ \cos(3\pi/8) : \cos(\pi/4) : \cos(\pi/8) : 1 : \cos(\pi/8) : \cos(\pi/4) : \cos(3\pi/8) \] between paths, which can be numerically approximated as \[ 1 : 1.8478 : 2.4142 : 2.6131 : 2.4142 : 1.8478 : 1 \].

B. Two-Stage 6P-HRM and 14P-HRM for TX

Both two-stage 6P-HRM [Fig. 3(a)] and 14P-HRM [Fig. 3(b)] involve gain weighting at BB and RF, phase rotation, and signal recombination. To resolve the gain mismatch, the selected gain ratios should be obtained via minimizing the cost function between the true and approximated values, while easing the circuit implementation.

For the two-stage 6P-HRM, the irrational gain ratio \[ \cos(\pi/4) : 1 : \cos(\pi/4) \] is realized half at BB with a pre-gain ratio \[ 2/5 : 3/5 : 2/5 \], and half at RF with a post-gain ratio \[ 4 : 5.6 : 4 \]. The 45° phase rotation is embodied into the mixers driven by an 8-phase LO. After all, the resultant gain ratio is \[ 29 : 41 : 29 \]. This approximation has \% relative error when compared to their true values. To be described later, such pre-gain ratio befits circuit realization in the BB LPFs, whereas the post-gain ratio minimizes the switching elements between 6P-HRM and 14P-HRM.

 Likewise, for the 14P-HRM, its irrational gain ratio \[ \cos(3\pi/8) : \cos(\pi/4) : \cos(\pi/8) : 1 : \cos(\pi/8) : \cos(\pi/4) : \cos(3\pi/8) \] is realized half at BB with a pre-gain ratio \[ 1/5 : 1/2 : 1/2 : 5/8 : 5/8 : 1/2 : 1/5 \] and half at RF with a post-gain ratio \[ 4 : 4 : 4 \]. The mixers driven by a 16-phase LO realize the 22.5° phase rotation. The resultant gain ratio \[ 1 : 1.8462 : 2.4134 : 2.6154 : 2.4134 : 1.8462 : 1 \] has < 0.1% relative error when compared with their true values.

C. Gain and Phase Mismatches of 6P-HRM and 14P-HRM

The intrinsic HRR of 6P-HRM and 14P-HRM can be compared in terms of random gain and phase mismatches. The concerned HRR expressions are summarized in Table I. \( \sigma_A \) and \( \sigma_\phi \)
are the standard deviations of the gain and phase mismatches, respectively. Note that the HRR has no difference between single-stage and two-stage HRMs. The only difference is on $\sigma_A$ [9]. Several HRR cases under different combinations of $\sigma_A$ and $\sigma_\phi$ are plotted in Fig. 3. The square-wave-like LO is based on a duty cycle $d$ of 50% for generality. As expected, the 14P-HRM rejects significantly more the seventh and ninth harmonics and is inherently more robust to gain mismatch. Section II-D describes the effectiveness of two-stage 6P-HRM and 14P-HRM in gain mismatch reduction.

**D. Gain Mismatch Reduction by Two-Stage 6P-HRM and 14P-HRM**

The gain mismatch of two-stage 6P-HRM can be derived using a vector diagram [Fig. 5(a)] similar to [9]. The three vectors in every circle have $45^\circ$ phase shifting for the first harmonic. The vector magnitudes represent the gain ratio of the first stage, whereas the multiplying factors represent the gain ratios of the second stage. Also, the vectors of adjacent circles have $45^\circ$ phase shift. The relative error of the first and second stages are denoted as $\epsilon_1$ and $\epsilon_2$, respectively. Every corresponding vector of the third harmonic has the same amplitude, but shifted by three times in phase. The two-stage approximated gain ratio of the first harmonic can be calculated as shown in Fig. 5(b). The total relative error of the third harmonic is given by (the subscript $2 - s$ implies a two-stage HRM)

$$
\epsilon_{2-s, 6P-HRM} = \frac{41 - 29\sqrt{2} + (21 - 15\sqrt{2})\alpha + (21 - 14\sqrt{2})\beta + 21\alpha\beta}{41 + 29\sqrt{2} + (21 + 15\sqrt{2})\alpha + (21 + 14\sqrt{2})\beta + 21\alpha\beta}
$$

which can be approximated as $1.49 \times 10^{-4} - 2.60 \times 10^{-3}\alpha - 1.46 \times 10^{-2}\beta + 0.256\alpha\beta$. This result is different from the derivation given in [9], since it uses $1/\sqrt{2}: 1$ as the gain ratio for both stages during the calculation, which does not match the practical circuit. In our model the exact gain ratios for both stages are adopted. In our derivation, the first term results from the approximation of the $\sqrt{2}$ by 41/29 and the second term appears from the gain mismatch of the first stage; both are negligibly small. The third term is determined by the gain mismatch of the second stage and it is suppressed by 68.5 times. The fourth term is even minor as it is the product of the first- and second-stage gain errors. Thus, the gain error after two-stage approximation becomes insignificant.

A similar vector diagram for two-stage 14P-HRM can be drawn [Fig. 6(a)]. There are seven vectors in every circle representing the seven gain ratios for every single path. Every adjacent vector has $22.5^\circ$ phase shifting. The two-stage approximated gain ratio of the first harmonic can be calculated as shown in Fig. 6(b). Under the same mismatch parameters as 6P-HRM, the total relative error of the third harmonic can be evaluated to be

$$
\epsilon_{2-s, 14P-HRM} = \frac{0.010 + 3.64\alpha + 5.08 \times 10^{-3}\beta + 1.8\alpha\beta}{27.17 + 6.23\alpha + 7.84\beta + 1.8\alpha\beta}
$$

which can be approximated as $3.78 \times 10^{-4} + 0.134\alpha + 1.87 \times 10^{-3}\beta + 6.62 \times 10^{-2}\alpha\beta$. It can be observed that the gain mismatch of the first stage is suppressed by 7.46 times while the gain mismatch of the second stage is almost cancelled.

**E. Comparison With the Two-Stage HRM in Receiver [9]**

As analyzed above, with the two-stage 6P-HRM and 14P-HRM, the gain mismatch becomes manageable. Recalling from Fig. 1, for a targeted HRR of 60 dB, the 6P-HRM (14P-HRM) should contribute just 36 dB (43 dB). Thus, the acceptable $3\sigma_\psi$ is relaxed to 3.6° (1.6°) for the 8-phase (16-phase) LO as plotted in Fig. 7, where $\sigma_A = 1\%$. Both are much relaxed when compared with [9], which entails 0.03° LO phase error to bear the
entire 60-dB HRR target. Thus, combining HRM with filtering in a TX should lead to significant power savings in the LO path. Moreover, as the HRR is mainly limited by the accuracy of the BB pre-gain ratios, the robustness of the two-stage HRM in TX should be better than that in receiver [9] (its pre-gain ratio is at RF).

IV. CIRCUIT IMPLEMENTATION

Fig. 8 depicts the detailed schematic of the proposed TX. The implementation is fully differential even it is exhibited as single-ended for brevity. The outputs of the upper and lower subband paths are combined at the DA, which should driver an off-chip power amplifier. The key building blocks are described below.

A. Codesign of BB LPF, Mixer Banks, and RF HRF

The first-stage gain ratio is embedded into the BB passive-RC LPF. Excellent matching over process variations is achieved via using a ratio of resistors: $R_2/(R_1 + R_2)$. The $-x2$-s-dB cutoff frequency $f_c$ is given by

$$f_c = \frac{1}{2\pi(R_1 + R_2)C_2}.$$  \hspace{1cm} (3)

For every path of the LPF, $C_1$ and $R_1/R_2$ are chosen to be 2 pF and 7.96 kΩ, respectively, such that a fixed cutoff frequency of 10 MHz can be set, minimizing also the phase mismatch at the BB. The phase rotation and frequency up-conversion are realized using a bank of active mixers, with each unit. Since the 14P-HRM only rejects harmonics up to the 13th, the RF HRF is designed to suppress the 15th harmonic by 36.5 dB to meet the 60-dB HRR target. It is a second-order passive-RC
network featuring four (65, 124, 235, and 456 MHz) and two (460 and 900 MHz) optimized cutoffs automatically selected with the LO for the lower and upper subbands, respectively. The effect of process variations and mismatches on HRR is assessed by Monte Carlo simulations. For instance, for a 65-MHz cutoff, the simulated standard deviation is 8.9 MHz. When transmitting a signal at 54 MHz (the toughest case), the corresponding HRR varies just ±1.3 dB, avoiding any calibration.

**B. Wideband DA With an Embedded CLC-Ladder BSF**

The schematic of the DA is depicted in Fig. 9(a). The segmented V-to-I input branches of the DA realize the required...
second-stage gain ratio. $M_1$ is source-degenerated by $R_dC_d$ to improve the passband flatness. The effective transconductance $g_{m, eff}$ is given by

$$g_{m, eff} = \frac{g_{m1}}{1 + g_{m1}R_d} \frac{1 + s2R_dC_d}{1 + s\frac{2R_dC_d}{1 + g_{m1}R_d}}$$

(4)

where $g_{m1}$ is the transconductance of $M_1$, and $R_d$ is the on-resistance of $M_1$, which also serves as a switch for changing the gain ratio at RF ($4 : 5.6 : 4 \leftrightarrow 4 : 3 : 4$), where only the mid branch has to be switchable. Although $5.6 \leftrightarrow 3$ is not integer-ratio switching, gain mismatch at the second stage is indeed minor (as analyzed in Section III-D and confirmed by simulations).

The DA uses a thick-oxide MOSFET as the cascade device to allow using a 2-V supply for better linearity. The combined output current is filtered in current mode by a third-order passive-CLC BSF. The frequency response of the BSF is given by

$$H_{BSF}(s) = \frac{1}{1 + s[2C_F1 + C_F2]g_{m2} + s^22C_F1L_F + s^34C_F1C_F2L_F/g_{m2}}$$

(5)

where $C_F1 = C_F2 = 2.37$ pF and $L_F = 4.5$ nH lead to a cutoff of 1.6 GHz. After accounting for the parasitic and package effects, the cutoff of the DA stays at 1.2 GHz. From Monte Carlo simulations, the 1.2-GHz cutoff can have a standard deviation of 71.4 MHz. When transmitting a signal at 432 MHz (the toughest case), the corresponding HRR$_3$ at 1.296 GHz varies just ±1.9 dB, which is acceptable without any calibration.

The overall frequency response of the DA can be derived as

$$H_{DA}(s) = \frac{v_{out}(s)}{v_i(s)} = \frac{g_{m1}Z_Fg_{m2}R_l}{2(1 + g_{m1}Z_d)(1 + s2C_F1Z_F + s^22C_F1L_F)}$$

(6)

where $g_{m2}$ is the transconductance of $M_2$, and $Z_d$ is the impedance of the $RC$ degeneration as given by

$$Z_d = \frac{R_d}{1 + s2R_dC_d}$$

(7)

Together with the package model, the simulated frequency responses of the DA with and without the BSF and $R_dC_d$-degeneration are compared in Fig. 9(b). It is clear that, without the BSF, the BW of the DA is excessive (~4 GHz), while the optimized response has small gain droop and shows a strong stopband rejection of around 65 dB/dec.
C. Wideband Low-LO_ref 8-/16-Phase LOG

Poly-phase LOGs are commonly based on dividers, necessitating a high-frequency reference LO to be supported by the frequency synthesizer. As analyzed before, the required $3\sigma_\phi$ of the eight-phase (16-phase) LO is relaxed to $3.6^\circ$ ($1.6^\circ$). Thus, the recently proposed injection-locked four-/eight-phase phase correctors (4PC/8PC) [11], [12] can be employed to relax the frequency and tuning range of the reference LO. The 4PC [Fig. 10(a)] and 8PC [Fig. 10(b)] are inverter-only circuitry. They are expandable, by cascading more of themselves, to optimize the phase accuracy.

The inverters are classified into three sets and two types: set A is for interpolating the intermediated phases. Set B is for natural-frequency suppression which leads to a larger operating frequency range. Set C is for signal injection and direct cascade of itself. For the two types, L-type stands for a larger device size than the S-type. The size ratio between L- and S-type inverters determines the locking range and the phase accuracy. A larger size ratio implies better phase-correcting ability but a smaller locking range. The phase-correcting ability of 4PC (8PC) can also be enhanced by cascading more of themselves,
at the expense of power. In post-layout simulations for a $1.0^\circ$ phase error, a cascade of five 4PC with $L/S = 3$ is minimum to progressively correct the phase error from $44^\circ \rightarrow 14^\circ \rightarrow 5.3^\circ \rightarrow 1.9^\circ \rightarrow 1.0^\circ$ at 432 MHz with a total power of 5.1 mW. Similarly, a cascade of six 8PC with $L/S = 3.75$ is minimum to correct the phase error from $52^\circ \rightarrow 11^\circ \rightarrow 4.4^\circ \rightarrow 2.1^\circ \rightarrow 1.2^\circ \rightarrow 1.0^\circ$ at 432 MHz with a total power of 6.0 mW.

The proposed 8-/16-phase LOG (Fig. 11) optimally combines different phase correctors and even-ratio-only frequency dividers to cover the entire TV band, allowing a low-frequency $\text{LO}_{\text{ref}}$ while offering appropriate 8- and 16-phase LOs for different frequency segments, i.e., 54 to 108 MHz, 108 to 216 MHz, 216 to 432 MHz, and 432 to 864 MHz. The $\text{LO}_{\text{ref}}$ is minimized to alleviate the design of a wideband synthesizer [13] when optimizing the power, VCO pulling, and tuning agility (a concern of CR for fast spectrum sensing). Moreover, the required division ratios for generating the 16-phase LO from 54 to 432 MHz are significantly reduced. All dividers in the layout are connected in a coiled manner [14] to equalize the delays between LO paths. The simulated frequency ranges of the four segments are 35 to 131 MHz, 70 to 263 MHz, 140 to 525 MHz, and 280 to 1160 MHz. The overlaps give sufficient margins for PVT variations.

The simulated LO phase error and the corresponding $3\sigma$-HRR are plotted in Fig. 12(a)–(d) for the four LO-frequency segments. The phase error starts to increase significantly at 486 MHz (lower subband) and 972 MHz (upper subband) due to the speed limitation of the LO buffers, which have two sets power-optimized for the upper and lower subbands. The worst in-band phase error of the eight-phase (16-phase) LOG is $1.17^\circ$ ($0.47^\circ$). Hence, the corresponding $3\sigma$-HRR of the 6P-HRM (14P-HRM) is $\sim36$ dB ($\sim44$ dB) for $\sigma_A \leq 1\%$. These results match to the targeted LO-phase accuracy (Fig. 1). Simulated under a noiseless $\text{LO}_{\text{REF}}$ over the TV band, the $\text{LO}_{\text{out}}$ shows $-152$ to $-128$ dBc/Hz phase noise at 1-MHz offset. The specifications of the frequency synthesizer can be referred to [7].

V. SIMULATION AND MEASUREMENT RESULTS

Prototypes of the TX were fabricated in 65-nm CMOS. The chip micrograph is shown in Fig. 13. The active die area is 0.93 mm$^2$, in which $\sim30\%$ is due to the BSF that has two on-chip inductors. The layout of the LOG is optimized for phase matching and is placed midway the 6P-HRM and 14P-HRM to simplify the LO distribution. The layout of multiple signal paths of 6P-HRM and 14P-HRM also affects the power efficiency. The simulated output power is dropped by 2 to 3 dB after $RC$ extraction. To perform statistical measurements over 16 available samples, a production test socket was utilized. The signal
A. Single-Tone and Two-Tone Tests

The single-tone tests measure the TX power efficiency, HRR, image-rejection ratio (IRR) and LO-rejection ratio (LRR), and are based on a 1 MHz BB differential I/Q signal, with its intrinsic dc and I/Q imbalances de-embedded out manually. With the output power measured to 2 dBm, the TX power efficiency is 0.42% to 1.19%, which is better than [7] (0.29% to 0.38%) and a multimode direct-digital TX [15] (0.07%). Fig. 15 plots the HRR, IRR, and LRR measured over 16 available dies. The worst HRR is 59.3 dB throughout the covered TV band. The ranges between 60 to 84.5 dB with 0.73 to 5.91 dB. The IRR features to 52.1 dB and 2.52 to 5.58 dB, whereas the LRR shows 42.7 to 48.8 dB and 2.31 to 5.09 dB.

Limited by the noise floor of the spectrum analyzer (−145 dBm/Hz, Rohde & Schwarz FSU8), the TX output noise was assessed by simulations. Referring to a −2 dBm single-tone output at 54 MHz, the TX shows a simulated in-band noise of −154 dBc/Hz at 60 MHz and −165 dBc/Hz at 864 MHz. The former is dominated by the buffers (40%) and BB LPFs (17%), whereas the latter is dominated by the buffers (70%) and DA (9%). Thanks to the BSF, the out-band noise reaches −175 dBc/Hz at 1.5 GHz (GPS band). To reach a +10-dBm output power at the antenna [7], a wideband power amplifier with a gain of 15 dB should be added.

A two-tone test assesses the output IP3 (OIP3). The injected two-tone BB signals are at 0.5 and 1 MHz. The measured OIP3 is +5.5 to +8.3 dBm over the covered TV band, which is affected by the insertion loss of the low-Q HRF and buffer. They show a simulated in-band gain loss of 2.5 dB at 54 MHz and 4 dB at 860 MHz, which in return entails a bigger signal swing from the mixers (simulated OIP3 = +1 dBm).

B. OFDM-Modulated Signal Tests

The consistency of the performances over the TV band is tested under a 6-MHz-BW 64-QAM 2048-point OFDM-modulated digital-TV signal, which has a peak-to-average power ratio of 17 dB and thus there is a 9-dB power back-off. A fixed BB signal is generated by the Agilent E4438C with a 96-MHz sampling rate for test at different frequencies. The output RF signal was captured in time domain and demodulated in MATLAB. The PSDs and constellation diagrams are plotted in Fig. 16(a)–(c).
TABLE II
CHIP SUMMARY AND BENCHMARK WITH THE STATE-OF-THE-ART HRM-BASED ARCHITECTURE

<table>
<thead>
<tr>
<th>Power (mW)</th>
<th>LO Path @ MHz</th>
<th>Total @ MHz</th>
<th>HRR (dB)</th>
<th>IRR/LR (dB)</th>
<th>EVM (@ MHz)</th>
<th>ACLR (dBc) @ MHz offset</th>
<th>Active Area (mm²)</th>
<th>Supply Voltage (V)</th>
<th>Technology</th>
</tr>
</thead>
<tbody>
<tr>
<td>This Work</td>
<td>2.5 @ 54</td>
<td>53.1 @ 54</td>
<td>&gt;59.3 (16 chips)</td>
<td>&gt;40.0 (16 chips)</td>
<td>2.8 @ 96</td>
<td>-46 @ 6</td>
<td>0.93</td>
<td>1.2 &amp; 2 (DA)</td>
<td>65nm CMOS</td>
</tr>
<tr>
<td>TMMT '11 [7]</td>
<td>14.2 @ 864</td>
<td>75.2 @ 864</td>
<td>Not Available</td>
<td>Not Available</td>
<td>4.0 @ 600</td>
<td>Not Available</td>
<td>2.5</td>
<td>1.8</td>
<td>0.8μm CMOS</td>
</tr>
<tr>
<td>ISSCC '06 [8]</td>
<td>Not Available</td>
<td>171 @ 54</td>
<td>&gt;42 (1 chip)</td>
<td>&gt;41 (1 chip)</td>
<td>Not Available</td>
<td>Not Available</td>
<td>0.14²</td>
<td>1.2</td>
<td>0.13μm CMOS</td>
</tr>
<tr>
<td>ISSCC '11 [9]</td>
<td>15.9 to 21.7</td>
<td>228 @ Not Available</td>
<td>&gt;40 (20 chips)</td>
<td>&gt;35 (1 chip)</td>
<td>Not Available</td>
<td>Not Available</td>
<td>1</td>
<td>1.2</td>
<td>65nm CMOS</td>
</tr>
<tr>
<td>ISSCC '11 [10]</td>
<td>Not Available</td>
<td>72</td>
<td>&gt;60 (40 chips)</td>
<td>Not Available</td>
<td>Not Available</td>
<td>Not Available</td>
<td>0.9</td>
<td>2.7 &amp; 1.3 (clock)</td>
<td>0.11μm CMOS</td>
</tr>
</tbody>
</table>

1 This work integrated a 3rd-order BSF. [7] and [8] have no BSF.
2 The area of the critical connection wires is excluded.
3 [7] boosts the single-tone output power to 10 dBm via an off-chip power amplifier that has a ~12-dB gain.

Note that the PSD noise floor and EVM accuracy were affected by the limited resolution (8 bits) of the oscilloscope (Agilent DSO91304A). Without any predistortion, the first (second) adjacent channel leakage ratio (ACLR) is −46 dBc (−43 dBc) at 6-MHz (12-MHz) offset. Both should be improvable by adding digital predistortion [16], harmonic cancellation [17], or linearization [18] to reach the IEEE 802.22 required ACLR of −46 dBc (−48 dBc), which should be assessed with the presence of the power amplifier. The measured EVM is 2.9% at 90 MHz, 3.3% at 384 MHz and 4.0% at 600 MHz; all are well below the IEEE 802.22 required 14%, allowing more EVM headroom for the power amplifier.

C. Performance Benchmarks

The chip summary and performance benchmark are given in Table II, this work is valuable for its: 1) low required I.O., 2) common BB inputs (differential and I/Q); 3) high power efficiency over the TV band; and 4) high-and-robust HRR achieved fully on chip.

VI. CONCLUSION

Design techniques and measurement results of a TV-band white-space TX have been described. The TX combines the wideband and robustness features of two-stage 6P-/14P-HRM, with the power and linearity benefits of passive-RC-/CLC filters, to manage the HRR fully on chip. Tested over 16 available 65-nm CMOS prototypes, the minimum HRR is 59.3 dB. The employed 8-/16-phase LOG is optimized via combining injection-locked 4PC/8PC and even-ratio frequency dividers. The LOG not only lowers the LO-path power (2.5 to 14.2 mW), but also the entailed reference LO frequency (432 to 864 MHz) that has been a common BW-bottleneck of most HRM-based architecture.

REFERENCES

RF circuits and systems for wireless, biomedical and physical chemistry, and engineering education. He has authored two books, Analog-Based Architectures and Circuits for Multistandard and Low-Voltage Wireless Transceivers (Springer, 2007) and High-/Mixed-Voltage Analog and RF Circuit Techniques for Nanoscale CMOS (Springer, 2012), and authored and coauthored over 120 papers in journals and conferences. He holds four U.S. patents.

Dr. Mak has served as appointed/elected member of the IEEE Circuits and Systems Society (CASS) Board-of-Governors (2007–2011), an associate editor of the IEEE Transactions on Circuits and Systems I—Regular Papers (2010–2011), the IEEE Transactions on Circuits and Systems II—Express Briefs (2011–2012), the IEEE Transactions on Information Theory Newsletter (2010–Present), and IEEE Potentials (2012–2014). He has served as a member of CASS Publication Activities (2009–2011), IEEE CASS CASCOM (2008–Present) and CASEO (2009–present) Technical Committees, Organization or Technical Committee Member of AVLSI’04, APCCAS’08, PrimeAsia’09–11, ISCAS’10, VLSI-SoC’11–12, RTI’11, SENSORS’11, APCCAS’12, A-SSCC’13 and ISCAS’15. He coinitiated the three short-term GOLD sessions in ISCAS09–ISCAS11. He was the recipient of the ASICON Student Paper Award 2003, the MWSCAS Student Paper Award 2004, the IEEE VLSI Workshop Best Paper Award 2004, the DAC/ISSCC Student Paper Award 2005, and the CASS Outstanding Young Author Award 2010. He was the (co)-recipient of the University of Cambridge Visiting Fellowship 2009, the IEEE MGA GOLD Achievement Award 2009, the CASS Chapter-of-the-Year Award 2009, the UM Research Staff Award 2010, the UM Academic Staff Award 2011, and the National Scientific and Technological Progress Award 2011. He was decorated with the Honorary Title of Value for scientific merits by the Macau Government in 2005.

Pui In Mak (S’08–SM’09–F’08) was born on April 30, 1957. He received the B.S., M.S., and Ph.D. degrees in electrical and electronic engineering from the University of California, Los Angeles, in 1980, 1985, and 1992, respectively.

Rui P. Martins (M’88–SM’99–F’08), born on April 30, 1957, received the B.S., M.S., and Ph.D. degrees in electrical and electronic engineering from the University of California, Los Angeles, in 1980, 1985, and 1992, respectively. He has been with the Department of Electrical and Computer Engineering (DECE)/IST, Technical University of Lisbon, Portugal, since October 1980. Since 1992, he has been on leave from Instituto Superior Técnico, Technical University of Lisbon, and is also with the Department of Electrical and Computer Engineering, Faculty of Science and Technology (FST), University of Madeira (UM), Funchal, Portugal, where he is a Full-Professor since 1998. At IST, he was the Dean of the Faculty from 1994 to 1997 and he has been Vice-Rector of the University of Macau since 1997. From September 2008, after the reform of the UM Charter, he was nominated after open international recruitment as Vice-Rector (Research) until August 31, 2013. Within the scope of his teaching and research activities, he has taught 21 bachelor and master courses and has supervised (or co-supervised) 26 theses, Ph.D. (11), and Masters (15). He has coauthored five books and coedited seven books, plus five book chapters, 266 refereed papers in scientific journals and conference proceedings, as well as other 70 academic works, for a total of 348 publications. He has also coauthored seven U.S. patents. He created the Analog and Mixed-Signal VLSI Research Laboratory of UM: http://www.ist.uma.mt/en/lab/ans_vlsi/web-site/index.html, elevated in January 2011 to State Key Lab of China (the 1st in Engineering in Macau), as its Founding Director.

Rui P. Martins was the Founding Chairman of the IEEE Macau Section from 2003 to 2005 and of the IEEE Macau Joint-Chapter on Circuits And Systems (CAS)/Communications (COM) from 2005 to 2008 [2009 World Chapter of the Year of the IEEE Circuits And Systems Society (CASS)]. He was the General Chair of the 2008 IEEE Asia-Pacific Conference on Circuits And Systems—APCCAS 2008, and was the Vice-President for the Region 10 (Asia, Australia, the Pacific) of the IEEE CASS, for the period of 2009 to 2011. He is now the Vice-President (World) Regional Activities and Membership also of the IEEE CASS for the period 2012 to 2013. He has been an associate editor of the IEEE TRANSACTIONS ON CIRCUITS AND SYSTEMS II: EXPRESS BRIEFS since 2010 and until the end of 2013. Plus, he is a member of the IEEE CASS Fellowship Evaluation Committee (Class of 2013). He was the recipient of two government decorations: the Medal of Professional Merit from Macao Government (Portuguese Administration) in 1999, and the Honorary Title of Value from Macao SAR Government (Chinese Administration) in 2001. In July 2010, he was elected unanimously as Corresponding Member of the Portuguese Academy of Sciences (in Lisbon), being the only Portuguese Academician living in Asia.

Ka-Fai Un (S’09) received the B.Sc. degree in electrical engineering from National Taiwan University, Taipei, Taiwan, in 2007, and the M.Sc. degree in electrical and electronics engineering from the University of Macau (UM), Macao, China, in 2009, where he is currently working toward the Ph.D. degree at the UM State-Key Laboratory of Analog and Mixed-Signal VLSI and Faculty of Science and Technology (ECE). His research interests are switched-capacitor circuits and wireless circuits design. Mr. Un won the Macau Mathematics Olympics in 2003 and represented Macau in the Chinese Mathematics Olympiads (CMO) and the International Mathematics Olympiads (IMO), in Changsha and Tokyo, respectively. He was the recipient of the 2008 APCCAS Merit Student Paper Certificate.

Ka-Fai Un (S’09) received the B.Sc. degree in electrical engineering from National Taiwan University, Taipei, Taiwan, in 2007, and the M.Sc. degree in electrical and electronics engineering from the University of Macau (UM), Macao, China, in 2009, where he is currently working toward the Ph.D. degree at the UM State-Key Laboratory of Analog and Mixed-Signal VLSI and Faculty of Science and Technology (ECE). His research interests are switched-capacitor circuits and wireless circuits design. Mr. Un won the Macau Mathematics Olympics in 2003 and represented Macau in the Chinese Mathematics Olympiads (CMO) and the International Mathematics Olympiads (IMO), in Changsha and Tokyo, respectively. He was the recipient of the 2008 APCCAS Merit Student Paper Certificate.

Pui-In Mak (S’00–M’08–SM’11) received the Ph.D. degree from University of Macau, Macao, China, in 2006.

Pui-In Mak (S’00–M’08–SM’11) received the Ph.D. degree from University of Macau, Macao, China, in 2006.

He is currently an Associate Professor with the University of Macau (UM), Macao, China. He has been with the UM State-Key Laboratory of Analog and Mixed-Signal VLSI as a Research Assistant (2003–2006), Invited Research Fellow (2006–2008), and Research Line Coordinator (2008–present) of wireless and biomedical areas. He held a short-term position with Chipidea Microelectronics (2003) and was a Visiting Fellow/ Scholar with the University of Cambridge, Cambridge, U.K. (2009), INESC-ID, Portugal (2009), and University of Pavia, Pavia, Italy (2010). His current research interests are on analog, mixed-signal and...