**Research Background**

Pipeled-SAR ADCs achieve higher resolution with excellent power-efficiency.

- **Pipeline ADC**
- **SAR ADC**
- **Pipelined-SAR ADC**

**ADC performance survey** (12bits, 100MHz)

- **Non-identities:**
  - Noise at 12b
  - Sampling distortions at 12b
  - Use open-loop amplifiers: stage-gain error

**Key Proposed Techniques**

- Propose a Merge-Residue-DAC operation in the 1st stage for better noise performance
- Propose a series-switches bootstrapped technique to improve the sampling linearity
- Propose a binary-searched stage-gain error (BSSGE) calibration technique, being fully integrated in the 2nd stage ADC with compact area

**Proposed Techniques**

Partial-Interleaved (Pi) Pipelined-SAR ADC architecture

**Design challenge:**

- **PI architecture** degrades SNR as kTC is determined by \(C_{DAC} \times f_{1/4} \text{of input Cap. in [Y.Zhu,VLSI'12]}\)

**Merged-Residue_DAC operation:** Achieved 40% noise suppression by enlarging \(C_{DAC} \times f_3/4 \text{of input Cap. Input Cap. remains minimum to satisfy the kTC noise only}\)

**Series-switches bootstrapped technique:** The sampling linearity is improved from -68dB to -87dB

**Partial-Interleaved (Pi) Pipelined-SAR ADC architecture**

- **1st-stage (2b/cycle operation)**
- **2nd-stage (1b/cycle operation)**

**Design challenge:**

- **PI switches made of transmission gate in [Y.Zhu,VLSI'12]** cause sampling nonlinearity

**BSSGE calibration:**

- Short Cal. Time (≈125ms): 5 binary-searched cycles
- Wider error coverage range: ±85% with Min. step≤±1.5%
- Compact area: Cal. logic & Cal-DAC embedded in 2nd-stage SAR ADC
- Input independent test signal: gen. by 1st-stage SAR ADC

**Measurement Results**

- **Normalized Frequency (MHz):** Measured F/T of digital output (decimated by 25)
- **Die chip photograph:** Core area (including gain & offsets) (m)² 0.068mm²

**Summary and Comparison**

<table>
<thead>
<tr>
<th>Architectures</th>
<th>Pipelined-SAR/Pipelined-SAR</th>
<th>Pipeline-SAR</th>
<th>SAR-Pipelined-SAR</th>
</tr>
</thead>
<tbody>
<tr>
<td>Technology (m)</td>
<td>28</td>
<td>40</td>
<td>65</td>
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<tr>
<td>Resolution (%)</td>
<td>12</td>
<td>12</td>
<td>12</td>
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<tr>
<td>Sampling Rate (MHz)</td>
<td>200</td>
<td>200</td>
<td>200</td>
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<tr>
<td>Supply Voltage (V)</td>
<td>0.9</td>
<td>1.1</td>
<td>1.2</td>
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<td>Power (mW)</td>
<td>2.3</td>
<td>4.96</td>
<td>11.9</td>
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<tr>
<td>SNDR(Ref=1ppm)</td>
<td>50.5</td>
<td>65.3</td>
<td>57.6</td>
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<tr>
<td>SNR(Ref=1ppm)</td>
<td>75</td>
<td>65.5</td>
<td>65</td>
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<tr>
<td>Fo2/PD (GHz)</td>
<td>8.87</td>
<td>29.7</td>
<td>92.8</td>
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<tr>
<td>Fo2/PD (GHz)</td>
<td>4.44</td>
<td>17.7</td>
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<td>Area (mm²)</td>
<td>0.1</td>
<td>0.042</td>
<td>0.048</td>
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<td>Gain Cal.</td>
<td>No</td>
<td>No</td>
<td>No</td>
</tr>
<tr>
<td>Gating Cal.</td>
<td>No</td>
<td>No</td>
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</table>

- Achieved compact area with all calibrations on-chip
- Achieved competitive performance for hi-res solutions & low power target