A 0.3-V, 37.5-nW 1.5~6.5-pF-Input-Range Supply Voltage Tolerant Capacitive Sensor Readout

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Abstract—A fully-digital capacitive sensor readout circuit based on capacitance controlled oscillators is presented. A two-step quantization scheme using SAR for coarse conversion and $\Delta \Sigma$ for fine conversion is introduced to extend the sensor input range while preserving the sensing accuracy. Systematic error analysis and optimization for the finite switch on-resistance and buffer input dependent delay are also outlined. Power supply insensitivity is ensured by the use of a pseudo-differential architecture and a ratiometric readout scheme. The complete sensor readout is implemented in a standard 0.18μm CMOS process. Simulation results show that the sensor readout circuit can achieve a wide input range from 1.5 to 6.5pF and a worst case power supply rejection ratio of 0.65% from 0.3V to 0.6V. For the $\Delta \Sigma$ conversion, a resolution of 7.4b at a conversion frequency of 318 Hz with an input capacitance of 4pF and a 0.3V supply is achieved. An average power is 37.5nW at 0.3V with a 4pF input capacitance, corresponding to a Figure-of-Merit (FoM) of 350fJ/conv-step.

I. INTRODUCTION

The limited energy capacity has always been one of the major bottlenecks in wireless sensing systems such as portable biomedical devices and wireless sensor networks [1]. To solve this problem, systems equipped with energy scavengers and ultra-low power high efficiency electronics are generally practiced to achieve system autonomous and extend system lifetime. Despite the advantages of energy harvesting systems, the environmental energy typically does not spread homogeneously. The temporal fluctuation induced supply noise and the low voltage generated (typically between 0.3V and 0.6V depends on different illumination conditions) present major challenges for designing a high accuracy sensor readout circuit with ultra-low power consumption using such energy source. This work focuses on the design of a capacitive sensor readout that can be powered directly by solar energy harvesters.

In [2], a ring-oscillator-based sensor readout circuit directly supplied by integrated photodiodes is demonstrated. Due to the strong dependency between the supply voltage and the oscillation frequency, large readout error exists under different illumination conditions, jeopardizing the system robustness. This supply variation issue is resolved in [3] by inserting a linear regulator to provide a stable supply voltage to the sensor readout circuit. However, this inevitably induces extra energy loss, penalizing the system energy efficiency. In [4], a high sensor readout accuracy is achieved by improving the supply insensitivity using a force-balanced Wheatstone bridge and differential Maneatis-cells. However, a relatively high minimum supply voltage of 0.85V is necessary and extra DC-DC conversion stages may be needed if it is powered by solar energy harvesters. In [5], a fully-digital capacitive sensor interface that can operate at a supply voltage down to 0.3V is presented. An estimated power supply rejection ratio (PSRR) of 1.2% is achieved by using a pseudo-differential architecture and a ratiometric readout scheme. However, this topology is sensitive to the variation in the sensor offset capacitance. It also has a narrow input sensing range (~300fF) due to the distortion and mismatch introduced in the readout paths, limiting its potential for application area.

This work presents a fully-digital two-step SAR/$\Delta \Sigma$ capacitive sensor readout with a wide input-range of 1.5–6.5pF. It can operate under a supply voltage from 0.3 to 0.6V, and can be directly powered by solar energy harvesters without extra DC-DC conversion. By using two capacitance-controlled-oscillators (CCOs) in pseudo-differential configuration and a ratiometric readout scheme, a PSRR of 0.65% within the targeted supply range is achieved. This paper is organized as follows. Section II outlines the proposed two-step wide-range sensor readout circuit architecture with a systemic error source analysis. Section III provides the simulation results of the proposed readout circuit using a standard 0.18μm CMOS technology. The conclusion is given in section IV.

II. SYSTEM OVERVIEW

A. Two-Step Capacitive Sensor Readout Architecture

Fig. 1 shows the block diagram of the proposed two-step capacitive sensor readout, which is composed of two
During the fine conversion, the capacitive sensor readout. Two inverter-based CCOs are constructed to cancel the sensor offset capacitance \( C_o \) and the \( \Delta \Sigma \) stage to convert the sensor residue capacitance \( C_{res} \). Fig. 2 shows a complete conversion cycle of the proposed capacitive sensor readout. At the beginning of the coarse conversion, the control logic first configures the converter into SAR mode (coarse conversion stage). During this period, the two CCOs perform capacitance-to-time conversion and generate two time signals \( T_s \) and \( T_r \) corresponding to the sensor capacitance \( C_s \) and the reference capacitance \( C_r \), respectively. Their phase difference is then determined and digitized by the phase detector. The generated digital output is then fed back to the SAR capacitor array to perform successive approximation. At the end of the coarse conversion, a 5-b digital output \( B_{SAR} \) results and is utilized in the following fine conversion stage. The control logic block controls \( B_{SAR} \) so that \( T_r \) should be strictly smaller than \( T_s \) to ensure proper \( \Delta \Sigma \) conversion, and configures the sensor readout into \( \Delta \Sigma \) mode to maximize hardware reuse. During the fine conversion, \( C_d \) is utilized for signal conversion and \( T_r \) switches to either \( T_{r1} \) or \( T_{r2} \) depending on the output bit in each cycle. The two CCOs act as time integrators to perform first-order noise-shaping. The output bitstream \( B_{\Delta \Sigma} \) can then be combined with \( B_{SAR} \) to generate the final digital output. This two-step conversion takes advantage of the fast SAR conversion and the high resolution \( \Delta \Sigma \) readout to achieve improved energy efficiency. The introduction of the SAR stage can also resolve the intrinsic limited sensing range as in a standalone \( \Delta \Sigma \) implementation, and will be discussed further in section II.B2.

B. Design Considerations

Fig. 3 shows the detailed implementation of the capacitive sensor readout. Two inverter-based CCOs are constructed using a signal conversion stage followed by buffers. The capacitive sensor \( C_s \) and the capacitive array are inserted within the corresponding signal conversion stage. The outputs from the CCOs are compared using a D-Flipflop (DFF) and the result is forwarded to the control logic for proper conversion operations. Even though the circuit can operate at ultra-low voltage operation for improved energy performance, this also limits the use of cascoding stages which can significantly jeopardize the PSRR of the capacitive sensor readout. The non-ideal effect of switch charge error have investigated in [8] and have solved by a new switching and calibration schemes. However according to our circuit the effect of increased switch impedance is a mainly limitation. Another detrimental effect on the sensor readout performance is the non-ideal buffer delay as a result of the low-supply voltage. This section investigates each of these non-ideal effects to achieve optimized sensor readout performance.

1) Switch Arrangements

Due to the finite on- and off-resistance of CMOS switches, the implementation and arrangement of the switches is imperative to improve the sensor readout performance. To reduce the input dependent switch resistance effect, all the switches are implemented using transmission gates. Fig. 4(a) shows two different switch arrangements SL1 an SL2 for capacitor selection, where the switches are arranged in two different configurations. With \( R_p \) and \( R_{tg} \) denote the average on resistance of a PMOS and transmission gate in the charging phase, respectively. Without loss of generality, we only consider the charging phase in the following analysis. During the charging period, the two voltages at the output nodes as shown in Fig. 4(a) are given by

\[ V_{SL1}(t) = V_{DD}(1 - \frac{R_p}{R_p + R_{tg}}e^{-t/\tau_{SL1}}) \]  

![Fig. 2. A complete conversion cycle of the proposed capacitive sensor readout: (a) Coarse SAR conversion stage; (b) Fine conversion stage.](image)

![Fig. 3. The detailed implementation of the capacitive sensor readout.](image)

![Fig. 4. (a) Switch location one (SL1) and switch location two (SL2) using transmission gate with charging phase equivalent model; (b) Delay vs. Cs, at different switch locations with changing switch widths.](image)
constant with buffer stage, respectively. Ideally, discharging phases for the signal conversion stage and the

It should be noted that the two switch arrangements deviate from the no switch case with decreasing signal delay can be achieved by using the SL2 and vice versa. SL1 and with SL2, respectively. It is shown that an increased power under the same power budget. Fig. 4. (b) shows the simulation result of the propagation delay without switch, with SL1 and with SL2, respectively. It is shown that an increased signal delay can be achieved by using the SL2 and vice versa. It should be noted that the two switch arrangements deviate from the no switch case with decreasing $R_{tg}$.

2) Buffer Stage Propagation Delay

Except from the signal conversion stage, the buffer stage which are implemented using even number of inverters, also generates finite delay that affect the CCO oscillation frequency ($f_{cco}$), which is defined as

$$f_{cco} = \frac{1}{t_{c} + t_{buf}}$$

where $t_{c}$ and $t_{buf}$ denote the total delay in both charging and discharging phases for the signal conversion stage and the buffer stage, respectively. Ideally, $t_{buf}$ should be the intrinsic delay which is signal independent. But as the input rise/fall time of the buffer stage deviates from the ideal step input, $t_{buf}$ becomes input signal dependent that can increase the signal distortion at the converter output, and affects both the $\Delta$C conversion. Fig. 5 illustrates the simulation result of the change in $t_{buf}$ as $C$ varies using the schematic as shown, and the dependency becomes significant as $C$ reduces. To solve this problem, $C_{dummy}$ with a value of 1.5pF is added in parallel to $C_{s}$ and $C_{r}$ as shown in Fig. 3. Using Fig. 5, to achieve an error of 0.5% with $\Delta C = \pm 150fF$, $C_{dummy} + C_{s,min}$ should be set to 3pF, and the corresponding $C_{LSB}$ and $C_{d}$ are set to 200fF and 300fF, respectively.

3) Power Supply Rejection

During the coarse detection, $C_{r}$ will approach $C_{o}$ and the residue error $C_{rd}$ is within 200fF. In order to avoid missing codes, $C_{d}$ is set to 300fF to introduce redundancy during the $\Delta$S operation. With $B_{1}$ denoting the ratio between the number of ones and the total number of bits in the $\Delta$S output bit stream, the following relationship between the oscillation frequencies of the sensor CCO and reference CCO can be obtained

$$\frac{1 - B_{1}}{f_{cco} |_{C_r=C_o}} + \frac{B_{1}}{f_{cco} |_{C_s=C_o+C_d}} = \frac{1}{f_{cco} |_{C_s}}$$

With a $C_{dummy}$ of 1.5pF and a worst case difference between $C_{r}$ and $C_{o}$ of 300fF, the result in $\Delta t_{buf} / t_{c}$ is within 0.5% (as illustrated in section II.B2), meaning that $t_{buf} |_{C_r=C_o} \approx t_{buf} |_{C_r=C_o+C_d} \approx t_{buf} |_{C_s}$ in the covered $\Delta$S sensing range. By using (6) and (7),

$$(1 - B_{1}) \times t_{c} = C_{o} + B_{1} \times t_{c} = C_{o} + C_{rd} = t_{c} = C_{o} + C_{rd}$$

The conversion stage delay of charging phase is given by (5). For any capacitor $C$, the corresponding time constant during the discharging phase is equal to $(R_{n} + R_{tg}) C$, and the total delay $t_{c}$ can be expressed as

\[t_{c} = \frac{2R_{p}}{R_{p} + R_{tg}} \ln \left(1 - e^{-t \cdot \frac{R_{p} + R_{tg}}{2R_{p}}} \right)
\]

Notice that the effect of $T_{G2}$ in Fig. 4(a), $S_{L2}$ is negligible as it is connected to a buffer with high input impedance.
As the equivalent resistance in (9) is sensitive to the supply voltage variation, $t_c$ is also prone to supply noise, resulting in a supply sensitive CCO output frequency. With a ratiometric readout scheme, the supply sensitive term can be effectively cancelled. By substituting (9) into (8),

$$C_{rd} = B_1 \times C_d \quad (10)$$

Theoretically, the power supply noise should be completely cancelled. However, the residues between different $t_{pf}$ and the mismatch in $R_p$, $R_n$ and $R_{tg}$ between the two CCOs can lead to finite PSRR. With the use of the coarse SAR conversion, the two CCOs can be better matched, improving the PSRR of the capacitive sensor readout. The use of a small $C_\alpha$ can also improve the linearity of the $\Delta \Sigma$ conversion, and the resolution is mainly limited by the phase noise of the CCOs [5].

### III. SIMULATION RESULTS

The complete capacitive sensor readout circuit is implemented using a 0.18μm standard CMOS process, with $C_\alpha$ ranging from 1.5pF to 6.5pF using a supply voltage of 0.3V. An Over-Sampling-Ratio (OSR) of 128 is used during the fine $\Delta \Sigma$ conversion. Fig. 6 shows the simulated INL of the two-step capacitive sensor readout. It can be observed that an INL of $\pm 0.5$ to $\pm 1.5$ LSB can be achieved in the entire input range, and is limited by the linearity and the capacitance mismatch of the two CCOs. Fig. 7(a) shows the simulated output spectrum with a mean input capacitance of 4pF and a peak-to-peak variation of 100fF at 62.1Hz. The sampling frequency and entire conversion frequency for the complete sensor readout are 81.4 kHz and 291 kHz, respectively. The calculated SNDR is 46.4dB, corresponding to a resolution of 7.4b. Fig. 7(b) shows the SNR/SNDR plot with the same settings using a mean input capacitance from 1.5pF to 6.5pF. It can be seen that the worst case occurs at minimum $C_\alpha$ as expected.

### TABLE I. PERFORMANCE COMPARISON

<table>
<thead>
<tr>
<th>Topology</th>
<th>$\Delta \Sigma$</th>
<th>$\Delta \Sigma$</th>
<th>SAR</th>
<th>PWM</th>
<th>SAR/\Delta \Sigma</th>
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<tr>
<td>Capacitive(C) / Resistive(R)</td>
<td>R</td>
<td>C</td>
<td>C</td>
<td>C</td>
<td>C</td>
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<tr>
<td>Sensor Range</td>
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<td>5.7–6 pF</td>
<td>50–53 pF</td>
<td>0.5–0.7 pF</td>
<td>1.5–6.5 pF</td>
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<td>Supply Voltage (V)</td>
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<td>1.4</td>
<td>3</td>
<td>0.3–0.6</td>
</tr>
<tr>
<td>ENOB</td>
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<td>6.1b</td>
<td>6.8b</td>
<td>8b</td>
<td>7.4b(1)</td>
</tr>
<tr>
<td>Power (μW)</td>
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<td>0.27</td>
<td>236.6</td>
<td>84</td>
<td>0.0375(1)</td>
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<td>Conversion Freq.(Hz)</td>
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<td>1k</td>
<td>0.26M</td>
<td>30k</td>
<td>318(1)</td>
</tr>
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<td>PSRR@DC</td>
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<td>1.2%(2)</td>
<td>-</td>
<td>-</td>
<td>0.65%(1)</td>
</tr>
<tr>
<td>FoM (pJ/conv-step)</td>
<td>13.03</td>
<td>3.9</td>
<td>7.9</td>
<td>10</td>
<td>0.35(1)</td>
</tr>
</tbody>
</table>

(1) Simulation result at 300mV supply with $C_\alpha = 4pF (\Delta \Sigma$ only).

(2) Estimated from the corresponding paper.

(3) Worst case over the entire sensing range.

$$t_c = \left( R_p + R_n + 2R_{tg}\right)C \ln 2 \quad (9).$$

As the equivalent resistance in (9) is sensitive to the supply voltage variation, $t_c$ is also prone to supply noise, resulting in a supply sensitive CCO output frequency. With a ratiometric readout scheme, the supply sensitive term can be effectively cancelled. By substituting (9) into (8),

$$C_{rd} = B_1 \times C_d \quad (10).$$

### IV. CONCLUSION

A fully-digital capacitive sensor readout circuit with wide input-range of 1.5–6.5pF that can operate with a supply voltage of as low as 0.3V in 0.18μm CMOS is presented. Non-idealities including the switch resistance and buffer stage propagation delay and their effect on the sensor readout performance are systematically analyzed. Simulation results show by using time-based pseudo-differential CCOs and ratiometric readout scheme, a PSRR of 0.65% from 0.3V to 0.6V is achieved. The sensor readout circuit consumes an average power of 37.5nW at 0.3V supply, and the achieved FoM for the $\Delta \Sigma$ conversion stage is 350fJ/conv.

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REFERENCES


