9.4 A 0.5V 1.15mW 0.2mm² Sub-GHz ZigBee Receiver Supporting 433/860/915/960MHz ISM Bands with Zero External Components

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The rapid proliferation of Internet of Things has urged the development of ultra-low-power (ULP) radios at the lowest possible cost, while being universal for worldwide markets. Both current-reuse [1,2] and ultra-low-voltage [3] receivers are promising solutions. [1] unifies most RF-to-BB functions in one cell for current-mode signal processing, resulting in a high IIP3 (~6dBm) at small power (2.7mW) and area (0.3mm²). However, outside the current-reuse cell, another supply is required for other circuits, complicating the power management [1,2]. [3] facilitates single-0.3V operation of the entire receiver at 1.6mW for energy harvesting, but the limited voltage headroom and transistor $f_I$ call for bulky inductors/transformers to assist the biasing and to tune out the parasitics, penalizing the IIP3 (~21.5dBm) and area (2.5mm²). In both cases, a fixed LC network was adopted for input matching and pre-gain to lower the NF, which is costly and inflexible for multi-band designs.

Aiming for a single-0.5V ULP receiver for sub-GHz ZigBee (IEEE 802.15.4/c/d) products (e.g., [4]), three circuit techniques are proposed: 1) An RF-to-BB-recycled front-end concurrently amplifies the RF (in common mode) and BB (in differential mode) signals under the same set of gain stages, squeezing the power by frequency separation and signal orthogonality. 2) An N-path (N=4) tunable LNA, embedded into the front-end, realizes low-noise input impedance matching while offering area-efficient blocker filtering to enhance the out-of-band linearity. ii) The 4G m weakens the effect of $R_{sw}$ to enhance the out-of-band linearity. iii) A VCO with extensively-distributed negative-gain cells for matching while offering area-efficient blocker filtering to enhance the out-of-band tunable LNA, embedded into the front-end, realizes low-noise input impedance matching while offering area-efficient blocker filtering to enhance the out-of-band linearity.

The receiver was fabricated in 65nm CMOS. Measurements (Fig. 9.4.4) showed that the gain (50±0.6dB) and IRR (20.5±1.7dB) are stable over the four ISM bands. A two-tone test at $[f_{LO}+12MHz, f_{LO}+22MHz]$ shows an IIP3 of ~20.5±1.7dBm. All $S_{11}$ are <-8dB and the VCO phase noise is ~117.4±1.7dBc/Hz at 3.5MHz offset. Owing to the merged VCO filter, the BB signal is ~50Vp-p, for not degrading the phase noise by 1dB. The 2MHz IF gain response shows 18/38dB rejection at the adjacent/alternate channel. Other results (not shown) are the out-of-band $P_{1db}$ (~20dBm), and blocker-NF (13.7dB) for a single-tone blocker of ~20dBm applied at 50MHz offset from the 860MHz RF. This blocker resilience is reasonably high for 1.15mW receiver power at 0.5V.

Benchmarking with the recent art [1,3,7] in Fig. 9.4.6, this work succeeds in covering multi-ISM bands with LO-defined input matching and RF filtering, while advancing the power and area efficiencies with zero external components. Figure 9.4.7 shows the die micrograph of the receiver.

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References:

Figure 9.4.1: Proposed RF-to-BB-recycled front-end.

Figure 9.4.2: Functional view of the RF-to-BB-recycled front-end. The memory effects of $C_i$ and $C_o$ associated with the 4-path SC network are detailed in Fig. 9.4.3.

Figure 9.4.3: a) An equivalent 4-path tunable LNA embedded inside the front-end. a) and b) are mathematically equivalent and modeled as c). d) The filtering profiles of c).

Figure 9.4.4: 0.5V current-reuse VCO filter and LO generation.

Figure 9.4.5: Measured key performance metrics.

Figure 9.4.6: Chip summary and benchmark with the state-of-the-art.
Figure 9.4.7: Die micrograph of the fabricated receiver.