Nanoscale CMOS offers sufficiently high \( f_t \) and low \( V_t \), favoring the design of ultra-low-power wireless receivers (RX) via stacking the RF-to-BB functions in one cell, while sharing the smallest possible bias current. Also, the signals can be conveyed in the current domain to enhance the area efficiency (i.e., no AC-coupling capacitor), RF bandwidth and linearity at those inner nodes. The 2.4-GHz LMM cell [1] for ZigBee RX is an example that unifies one LNA, two mixers (I/Q) and one VCO. The power is low (2.4-mW), but the NF, gain and \( S_{11} \) are sensitive to its external high-Q inductor that performs narrowband input match and passive gain boost. Although one VCO (i.e., one inductor) can save area and power, the I/Q generator has to be placed in the RF path. Realized as a \( Q \)-gate circuit, it suffers from a 3dB gain loss deteriorating the RX NF (12dB), while rendering the I/Q accuracy more susceptible to process variation.

The QLMM cell [2] for GPS RX facilitates I/Q generation via adopting a VQCO. Although its power is further optimized (1mW), three on-chip inductors and one off-chip balun are entailed, penalizing both die area and cost. In any case, both LMM and QLMM cells only can generate a 50%-duty-cycle LO for the mixing, which is less effective than its 25%-duty-cycle counterpart in terms of gain (i.e., 3dB higher), NF and I/Q isolation [3]. Finally, as their channel selection and image rejection are out of their current-reuse paths, any on-chip balun will be converted into the voltage domain before adequate filtering, constituting a hard tradeoff between noise, linearity and power (i.e., 1.2mW BB power in [1] and 5.2mW BB power in [2]).

This paper describes a zero-extreme-component 2.4GHz ZigBee RX (Fig. 25.5.1) with 1.7mW RF-to-BB power and 0.22mm\(^2\) active area. The RF signal (\( V_{RF} \)) is pre-gained by a low-Q passive network to ensure a wideband \( S_{11} \). A Blixer (Balan-LNA plus I/Q mixers) amplifies and downconverts the current signal to a 2MHz IF. Output-channel blockers are immediately filtered in the current domain by a hybrid filter, which is stacked atop the Blixer for current reuse. A non-asymmetrical high-swing VGA drives a 3-stage RC-RR polyphase filter (PPF) for robust image rejection. The final stage is an inverter amplifier. An LO generator creates a 25%-duty-cycle 4-phase output using a wideband div-by-2 (DIV1) and an external reference LO (\( L_{REF} \)). A div-by-4 (DIV1+DIV2) and a 100GHz VCO are also integrated for additional testability.

The Blixer (Fig. 25.5.2) features a passive-active-gain-boosting technique. The passive part is based on a low-Q and compact (0.048\( \mu \)m\(^2\)) 4.16\( \mu \)H inductor \( L_{a} \) and tapped capacitors \( C_{p} \) and \( C_{M} \) for impedance downconversion and resonance. \( L_{a} \) also serves as the bias inductor for \( M_{1} \). \( C_{p} \) stands for the parasitic node impedance of \( M_{F1}-M_{F2} \). At high frequency, the pole \( \frac{1}{g_{m1}C_{p}} \) of the \( M_{1}-M_{p} \)'s noise is absorbed to \( C_{p} \).

Unlike the original Blixer [3] that uses an RC load, the proposed “load” synthesizes a 1-order complex pole (Fig. 25.5.4). \( R_{p} \) comes from the diode-connected \( M_{1} \) realizing the real part, and \( g_{m1C_{p}} \) comes from the I/Q-cross-connected \( M_{1} \) realizing the imaginary part. Together with the Blixer (Fig. 25.5.3), 3-order channel selection and 1-order image rejection are achieved. \( M_{1} \) and a segmented \( M_{VGA} \) also act as a current-mirror VGA handling the NF and linearity of the BB circuitry. Since the current-mode Blixer (Fig. 25.5.3) already offers two poles, the linearity of the VGA is relaxed. Outside the current-reuse path, the BB circuitry further implements the image rejection (>50dB in corner simulations) and signal amplification. Thanks to the small span \( (\tau_{input}/\tau_{out})=3 \) of the image band, large resistors (~150k\( \Omega \)) and small capacitors (~0.47pF) are allowed in the PPF to save area.

The RX, fabricated in 65nm CMOS is optimized at 0.6V and 1.2V supplies. Since there is no frequency synthesizer, the results in Fig. 25.5.5 were measured under \( L_{REF} \). The –10dB \( S_{11} \)-BW is –1.3GHz in packaged and chip-on-board tests. Thus, both gain (55 to 57dB) and NF (8.3 to 11.3dB) are wide at RF, more immune to process variations. A two-tone test at [LO+12MHz, LO+22MHz] shows an IP3 of ~6dBm at a maximum gain of 57dB. The asymmetric IF response shows 22dB (43dB) rejection at the adjacent (alternate) channel, and 36dB IRR.

The chip summary is given in Fig. 25.5.6. The results obtained under a free-running 10GHz on-chip VCO are also included, but they are more sensitive to test uncertainties. Benchmarking with the prior art [1,2,6], this work succeeds in advancing the IP3, power and area efficiencies, while offering a wideband \( S_{11} \) with zero external component. Fig. 25.5.7 shows the die micrograph.

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References:


Figure 25.5.1: A 2.4GHz ZigBee RX.

Figure 25.5.2: Blixer and LO generator.

Figure 25.5.3: IF-noise-shaping Biquad. The \( L_{\text{act}}c_{\text{eff}} \) resonance shifts the noise-shaping zero to the 2MHz IF.

Figure 25.5.4: Complex-pole load. Upper: Block diagram. Lower: Schematic. \( M_L \) and \( M_{\text{VGA}} \) also form a current-mirror VGA.

Figure 25.5.5: Measured: \( S_{11} \), Gain and NF, IIP3, IRR and IF gain response.

Figure 25.5.6: Chip summary and performance benchmarks.

*The frequency synthesizer is already excluded for fair comparison.
Figure 25.5.7: The RX die photo.