A High-Voltage-Enabled Recycling Folded Cascode OpAmp for Nanoscale CMOS Technologies

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Abstract
This paper describes a high-voltage-enabling circuit technique for enhancing the gain precision and linearity of OpAmp-based analog circuits. Without resorting from specialized devices, a 2xVDD-enabled recycling folded cascode (RFC) OpAmp optimized in 1V GP 65-nm CMOS achieves, when compared with its 1xVDD counterpart, 25-dB higher open-loop DC gain and 30-dB higher IM3 (in closed loop), under a similar power budget. These joint improvements save the need of a 2nd stage in the OpAmp when high precision and high linearity are the priorities. A voltage-conscious bias scheme and gate-drain-source engineering ensure that all devices are consistently operated within the reliability limits.

I. INTRODUCTION
Rapid downscaling of CMOS has led to more compact and faster analog circuits but with deteriorated linearity and accuracy due to the associated low-voltage constraints. The value of the supply voltage (VDD) predominantly defines the number of transistors that can be cascoded in an amplifier. Entered into the sub-1V nanoscale regime, the downsizing of threshold voltage (VT) is decelerated due to variability, matching and leakage issues. Insufficient voltage headroom makes stacking of transistors no longer efficient. Cascading of transistors, on the other hand, demand more power and achieve lower operating speed. Innovative techniques befitting sub-1V nanoscale processes must be investigated in order to keep driving up circuit performances along with technology advancements.

Thus, instead of blindly tracking the downsizing of VDD in technology scaling, VDD-elevated analog circuits with design for reliability have emerged as a prospective circuit solution [1, 2]. An elevated VDD directly opens up much more voltage headroom (Fig. 1), while maintaining the speed and area benefits of fine linewidth processes.

In this paper, a high-voltage-enabling circuit technique is proposed for realizing a 2xVDD-enabled recycling folded cascode (RFC) OpAmp. Without resorting from a two-stage or multi-stage OpAmp, this new RFC OpAmp can offer sufficient open-loop gain to realize high-precision and high-linearity analog functions, when they are the priorities. The reliability of the circuit is ensured via voltage-conscious biasing and gate-drain-source engineering. It is worth to mention that the true value of 2xVDD is within 2 V at nanoscale CMOS, when VDD is roughly 1 V, which can be easily generated via a 3.6/3.7-V Li-ion battery in typical portable systems.

II. 1xVDD AND 2xVDD RFC OPAmps

A. Typical RFC OpAmp
The single-stage RFC OpAmp [3] is shown in Fig. 2. It is selected as the basis of our 2xVDD design for its high performances. The RFC OpAmp employs M1b, M2b, M11, M12, M3b and M4b to improve concurrently the gain and speed. By controlling the current mirror gain K, the small signal transconductance can be boosted, i.e., gmsRFC = gmsAll(1 + K). Thus, under a fixed power budget, the RFC shows a higher gain-bandwidth product (GBW) than the conventional folded cascode (FC) structure. Furthermore, the RFC OpAmp also exhibits larger output resistance than its FC counterpart, leading to further gain enhancement.

B. 2xVDD-Enabled RFC OpAmp with Design for Reliability
The proposed 2xVDD RFC OpAmp is depicted in Fig. 3. The aim of doubling the supply is to enhance certain performance metrics that cannot be simply obtained by doubling the bias current at 1xVDD under a similar power budget. By appropriately doing transistor stacking and biasing, the output resistance of the devices can be boosted while the voltage stress on them can also be shared to meet the reliability limits. For instance, under a 2xVDD, M0' can be added to share the voltage stress on the current source M0 and improve its output resistance, thereby the OpAmp’s common-mode rejection ratio (CMRR). On the other hand,
Degradation of MOS device characteristics occurs as a result of exposure to a high $V_{DS}$ with a large drain current. Examples of degradation are a shift of $V_{T}$ and a shorter gate-oxide breakdown lifetime. HCI normally happens in high-power circuits such as the power amplifier, where the worst HCI bias conditions: $V_{DS} \geq V_{GS} \geq V_{T}$ and $V_{DS} \geq V_{DD} / 2$ are concurrently satisfied. HCI degradation can be reduced by lowering the drain current or increasing the device oxide thickness ($T$) and channel length ($L$).
TDDB is the wear-out of insulating properties of silicon dioxide in the CMOS gate, leading to the formation of a conducting path through the oxide to the substrate. In order to protect the circuit against TDDB the catastrophic destruction of gate oxides induced by the maximum DC gate oxide voltage at different temperatures must be considered. According to the maximum DC gate oxide voltages of 65-nm CMOS, NMOS has a higher voltage standing capability than PMOS for all cases to prevent TDDB. Thus, NMOS is preferable when considering TDDB in circuit design.

BTI degradation happens under steady-state conditions. It is design dependent in analog circuits and primarily only PMOS devices are subjected to BTI stress, namely negative BTI (NBTI). In a VDD-Downscaled design, analyzing NBTI involves detecting, in all modes of operation (DC and small signal), which PMOS device is exposed to a peak or rms voltage value exceeding the standard $V_{dd}$, which is around 1 V in 65-nm CMOS. Thus, NMOS is also preferred in terms of BTI.

Complying with all of them in the design indeed translates the term design for reliability into voltage-conscious design, highly simplifying the design and verification methodologies [4]. Furthermore, in the topology formation phase, their implications to the circuits can be easily justified in circuit simulations as presented next.

The test circuit for assessing the performances of the 2xVDD RFC OpAmp is a 1st-order active-RC lowpass filter with unity gain, as shown in Fig. 5. To check the reliability of all devices inside the OpAmp, a large square-wave input at a common-mode voltage of 1 V is applied. Fig. 6 shows the $V_{gs}$-$V_{ds}$ relationship at an input swing of 1.2 Vp-p. Since the circuit is differential, we just show the half-circuit simulations as presented next.

$1.25V$ for $1.6$- and $2V$ inputs, respectively. According to the liftime targets discussed in [5], $V_{ds} > 1$ V may still be acceptable for some applications.

IV. SIMULATION RESULTS

In order to compare the performances between 1x$V_{dd}$ and 2x$V_{dd}$ RFC OpAmps fairly, two 1x$V_{dd}$ RFC OpAmps are designed. The power budget of the 1-V RFC OpAmp #1 is roughly half of the 2x$V_{dd}$ design, whereas the 1-V RFC OpAmp #2 consumes roughly the same power as the 2x$V_{dd}$ one. Designed in a 65-nm CMOS process with 1-V GP
design example, under a 2-V supply in 65-nm CMOS process, achieves 25-dB higher open-loop DC gain and 30-dB better IM3 (in closed loop) than its 1xVDD design even with the same power budget, as there is inefficient voltage headroom. A high-voltage-enabled OpAmp, hence, appears as a perspective solution that can enhance the gain precision, CMRR and linearity of analog functions in nanoscale CMOS with no extra manufacturing cost or reliability risk.

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REFERENCES